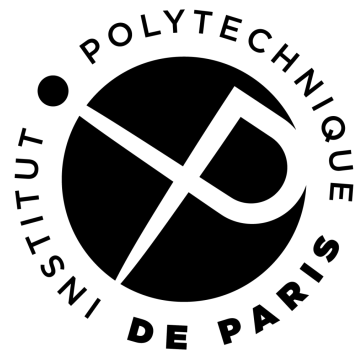


Advanced Programming of Multicore Architectures

Master in computer science of IP Paris

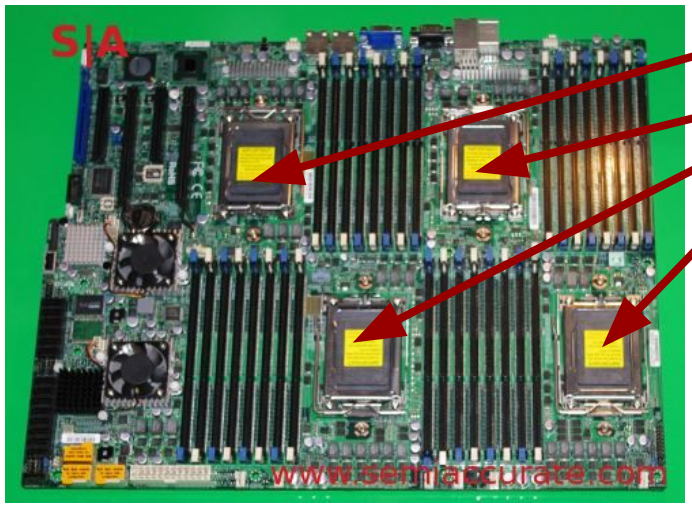
Master CHPS of Paris Saclay

Gaël Thomas

Multicore architectures

- Multicore architectures are today everywhere
  - Large multicores in data centers (up to 64/128 cores)
  - Small multicores in desktops or smartphones (up to 8/16 cores)

- Goal of the course: understand how we can program **at low level** a modern multicore architecture



arya.int-evry.fr
4 sockets with 12 cores in each socket
=> 48 cores in total

Organization

- 6 weeks with
  - 1h to 2h of theory
  - 4h to 5h of practice during labs
  - 1h in average of homework each week

- One subject each week
  - Threads and synchronization (mutex/varcond in course 1)
  - Lock algorithms (course 2)
  - Non-blocking algorithms (course 3)
  - Transactional memory (course 4)
  - Non-uniform memory architectures (course 5)
  - Non-volatile memory (course 6)

Prerequisites

- Good programming skills in C
  - Pointers, memory management
- Some background in systems
  - Notion of process and inter-process communication