

Leveraging a user-land page table to efficiently use modern memory

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1 Context

The upcoming launch of CXL [26] will profoundly impact resource management in a data center. CXL defines a cache-coherent protocol at the scale of a whole machine. The cache-coherency domain includes the PCIe devices, the system memory and the CPUs. CXL opens the way to a fully disaggregated data center because we can connect the PCIe buses of a cluster of machines to a CXL fabric [11, 14]. In this setting, the loads and stores emitted by a processor are routed to the CXL fabric through the PCIe bus of the emitter, and then to the PCIe bus and the memory of the receiver. At the software level, accessing a local or a *far* memory located in another machine becomes thus totally transparent since an expression as simple as `a = 42` can be routed transparently to any memory of any machine connected to the CXL fabric.

Additionally to transparency, CXL also brings efficiency. First experiments report a far memory access latency that ranges from 300ns to 600ns [14, 26] : roughly 10 times faster than sending a page via RDMA [12, 23], and only 1.5 to 3 times slower than an access to a memory located in another domain on a Non-Uniform Memory Access (NUMA) architecture.

In this context, the old n-tier design that has dominated for thirty years become inadequate. The n-tier design allows the computation and the storage to scale independently, but induces a high cost because of data exchange between the tiers. This data exchange requires data transformations, which annihilates the advantage of an optimized cache-coherency protocol at the scale of a cluster of machines.

2 Subject

In the DiVa project of the PEPR Cloud, we have the goal of rethinking the architecture of the cloud applications at the era of CXL. For that, we propose to decouple the memory from the process. In detail, as in a multi-threaded setting, we propose to consider a global memory pool, and a set of processes that act on the memory pool. However, contrarily to a classical multi-threaded setting, the memory exists regardless of the processes : the memory acts as a permanent storage for ephemeral processes, which are launched on demand to serve clients or to perform large data analytics. Because any process can directly access the global memory, the architecture avoids the high cost of transforming data when it is exchanged between the processes.

Central to this architecture is a naming service, which, at a high-level, comes in replacement of a classical file system. This naming service has to allow a process to retrieve an object produced by another process from an identifier. The research project has the goal of studying how we can design such a naming service (a map) in shared memory able to scale to thousands of processes. For that, we will study how we can reuse a memory management unit to accelerate the access to the naming service.

3 Advisors expertise

Gaël Thomas (Benagil team) is an expert in systems. He has been working on NUMA architectures [4, 9, 10, 28], privacy [25, 29], performance analysis [5, 17], persistent memory [6, 13], concurrent programming [15, 16, 21, 22], bug analysis [19, 20, 24], and language runtime designs [1, 7, 8, 27]. Jana Toljaga (Banegil team) is a PhD candidate expert in virtualization and operating systems.

4 Expected skills

The candidate must have a good background in system programming, concurrent programming, distributed systems and C/C++.

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